GCST

1.1 SYSTEMS ARCHITECTURE

TOPIC WISE EXAM QUESTIONS

ANSWERS

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2023

1 mark for example: e.g. • Auto lights • Auto window wipers • Sat nav // GPS • Airconditioning // climate control • Radio/entertainment/infotainment system/media system • Lane assist • Engine management system • Auto-park • Cruise control • Auto-brake • Follow-me • Dashcam 1 mark each to max 2 for explanation. • **Limited** functions // by example e.g. the system **only** checks the light and turns lights on/off • **Dedicated** microprocessor // by example e.g. there is a microprocessor that is only checking the lights • Hard to change function // by example e.g. the user cannot make the light system do any other role	3	Allow anything that could be reasonably within a car. If example is not clear if it's an embedded system, read explanation for justification e.g. hazard lights – could be embedded if they are activated automatically when the car crashes. Award the example in the explanation if this occurs. If justification is generic features of an embedded system max 1 for explanation. Do not award 'built into the car/larger machine' because this is in the question.

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2022

Question	Answer	Mark	Guidance
2	1 mark for each term or definition **CPU component or register** / **Definition** Program Counter // PC: Stores the address of the next instruction to be fetched from memory. Increments in each fetch-execute cycle. CU (Control Unit): (Sends signals to) **synchronise** / **control** / **coordinates** the processor/hardware/F-E cycle/processes/**flow** of data // **decodes** instructions (in CIR) // **runs** F-E cycle Memory Address Register // MAR: Stores the address of the data to be fetched from, or the address where the data is to be stored. Arithmetic Logic Unit // ALU: Performs the mathematical and logical calculations.	4	Read whole answer for CU and award correct point at any stage. CU 'sends signals to components' is not enough, it isn't saying what the signal's purpose is

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SAMPLE

1	a		It has more cores.	1 (AO2 1a)	Although Computer 1 has a lower clock speed than the CPU in Computer 2 it has more cores, which means that it can be faster than Computer 2. Any answer relating to splitting a program into processes that be carried out consecutively will be accepted.
1	b		RAM SSD HDD Graphics card (GPU)	2 (AO2 1a)	Marks can be awarded for other appropriate responses: e.g. Motherboard Sound card
1	c		• data is transferred faster (1)… • …which makes a CPU more efficient (1) • It is faster to transfer to and from cache (1)… • …than transferring to and from RAM (1).	2 (AO2 1a)	1 mark to be awarded for each correct identification and 1 mark to be awarded for the associated explanation to a maximum of 2 marks.
1	d		• An instruction is fetched from memory • The instruction is then decoded • The decoded instruction is then executed so that the CPU performs continuously • The process is repeated • The program counter is incremented • The instruction is transferred to the MDR • The address of the instruction to be fetched is placed in the MAR	2 (AO1 1a)	1 mark to be awarded for each correct answer to a maximum of 2 marks.

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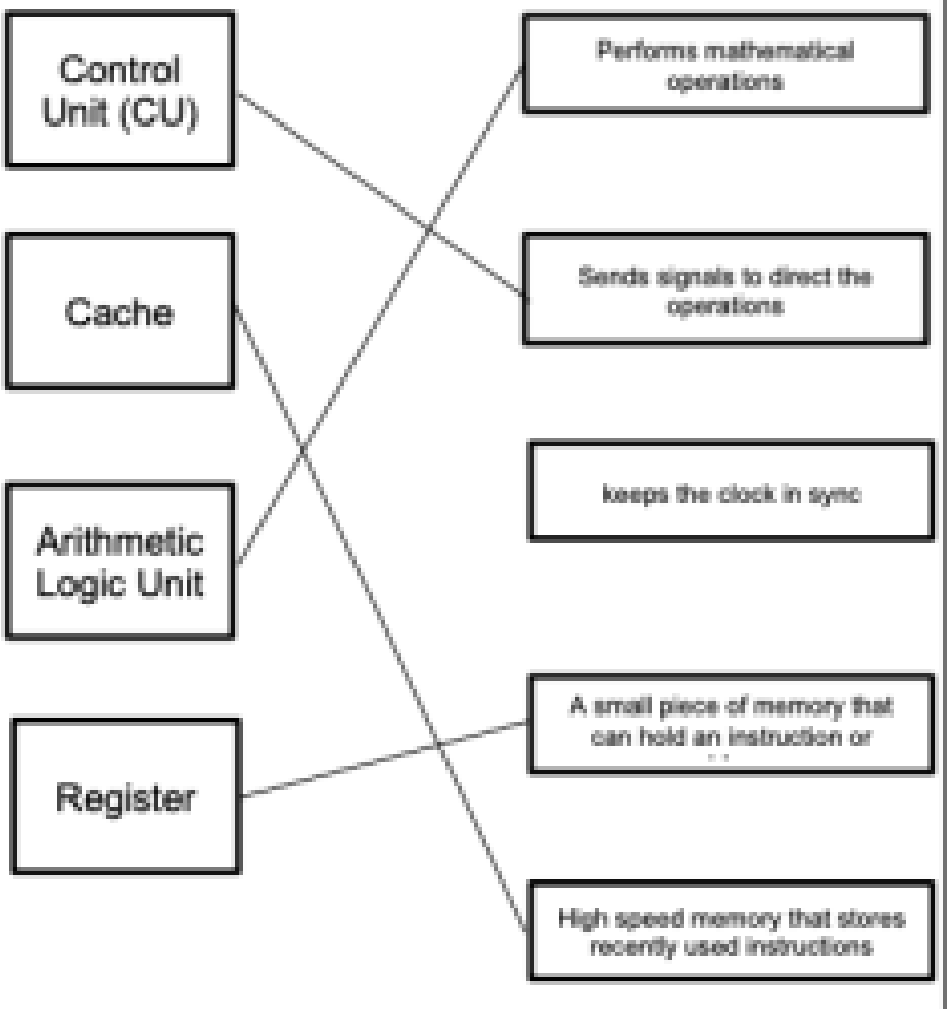
2021

1	b	(i)	• CPU performs the FDE cycle • Process **instructions**	1	
		(ii)	1 mark per bullet to max 2 • Single core means there is only **one processor** • 2.5Ghz means it can run 2.5 billion FDE cycles per second	2	MP1 BOD single processor Allow instructions for MP2
1	c		1 mark each • PC • MAR • MDR • Accumulator	2	Accept other correct registers (e.g. CIR, IR) Read first answer on each line

2020

3			1 mark per correct line from component to definition	4



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2019

1	a	i	1 mark for each completed word CPU stands for **Central Processing Unit**. It is the part of the computer that fetches and executes the **instructions** that are stored in **(main) memory**. The CPU contains the Arithmetic **Logic** Unit (ALU) and the **Control** Unit (CU).	5 AO1 1a (5)	Accept: • RAM/registers in place of "memory" • bod cache/MDR/CIR in place of memory • 'and Logic' in place of Logic • ignore 'data' if they put 'data and instructions' but no mark for data on its own • Do not award command for instructions • Bod central processor unit • Bod logical
1	a	ii	1 mark per bullet to max 2 • Dual core is 2 processors/cores // double the number of processors/cores • Parallel processing can take place • … which means each processor can execute a separate instruction **at the same time** // each processor can run a different part of the program **at the same time** // each core can process instructions **independently** of each other • ...which enables multitasking • Some processes/software **cannot** be split between two processors so it does not increase the performance	2 AO1 1b (1) AO2 1b (1)	• Needs the notion of the processors acting at the same time i.e. not just 'it can run twice as many instructions' without 'at the same time'. • Do not award more instructions per second - this could be achieved by having a faster clock speed. • Allow FDE for 'executing instructions'. • Do not allow 'cores can split the tasks' – need to be how i.e. one task for each core to run at the same time. • BOD run more than one program at once
1	a	iii	1 mark per bullet to max 2 • Cache stores frequently/recently/next to be used instructions/data • …that can be **accessed** faster than **accessing** them from RAM • …which means more cache improves the performance of the CPU // less cache decreases the performance of the CPU • Too much cache can be detrimental … • …as it will take longer to find the instructions in cache	2 AO1 1b (2)	• No mark for just defining cache as being fast memory or close to the CPU. • No mark for cache is faster than RAM - faster at what? • Bod - More cache makes the processing faster • Bod - More cache makes the computer run faster
2	c	i	Smart watch	1 AO2 1a (1)	CAO
2	c	ii	1 mark per bullet for justification to max 2 • A smart watch is not a general-purpose computer • … which means the smart watch has one/limited/specific/dedicated function(s) • Smart watch has a microprocessor • … on a single circuit board • It is a computer system that is built within the watch • Runs firmware • Smart watch has built-in OS // difficult to change/manipulate the OS/function • Smart watch has few components all essential to its purpose • Smart watch has specific hardware required to function i.e. speaker/headphones	2 AO2 1b (2)	• Answers must be applied to scenario. Do not award generic definitions. • Allow opposite reasons for why a laptop is not an embedded system but do not allow repeated points.

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2018

4	(a)		1 mark per bullet to max 2 per register
			• MAR // memory address register
			• Stores the address/location where data will be **read/written/accessed/fetched**
			// address/location of data/instruction being **processed**
			// address/location of data/instruction next to be **processed**
			
			• MDR // memory data register
			• Stores the data/instruction that is **fetched/read** from memory
			// stores the data that is to be written to memory
			// stores the data/instruction from the address in the MAR
			// data/instruction next to be **processed**
			
			• Program counter
			• Stores the address/location of the next instruction to be run
			// stores the address/location of the current instruction being run
			
			• Accumulator
			• Stores the result of manipulation/process/calculation
				4
				AO1 1a (2)
				AO1 1b (2)
					MAR stores address is not enough for description
					MDR stores the data is not enough for description
					
					Allow:
					• Current instruction register // IR
					• Stores the instruction currently being processed
					
					Accept MBR // Memory buffer register for MDR

4	(b)		1 mark per bullet to max 2 • The number of FDE cycles run per given time/second // the frequency that the clock 'ticks' • 3.8 billion cycles/instructions … • …per second	2 AO1 1b (1) AO2 1a (1)	Do not award: how fast the computer is // speed of CPU 3.8 = 3,800,000,000

4	(c)		1 mark per bullet to max 3
			e.g.
			• Software may be designed to run on 1 core and not multiple cores
			// depends on the task(s)
			• …some tasks cannot be split across cores
			• Clock speed also affects speed
			// dual core may have a faster clock speed
			// quad-core may have slower clock speed
			• ….so one task may be run faster/slower
			• RAM size also affects speed
			// Quad-core may have less RAM
			// amount of VM being used
			• Cache size also affects speed
			// Quad-core may have less cache
				3
				AO1 1b (1)
				AO2 2b (2)
					Allow marks for other components that could affect the speed e.g. secondary storage access speed, onboard GPU.
					Award description of concurrent processing.

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2016

6	a	2 from • Tasks can split between the processors… • …tasks/processes/software/ can be processed faster • …more processes completed per second • Allows multitasking // Run more than one process/task/instruction/data at a time/per clock cycle… • … tasks/processes/software/ can be processed faster • …more processes completed per second	2	MUST have given splitting tasks, or multi-tasking to allow speed Faster can only be given a mark if the first bullet(s) have been given.

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EXTRA

b		• To store instructions/data that is frequently used / previously used / next to be used • Data does not need to be fetched from RAM • Speeds up access	2

i	–Is needed to store the address of the next instruction (to be processed) –Value is then sent to the MAR –After sending the value the PC is incremented / changed to address held in CIR if the operation is a Jump	2	**Examiner's Comments** Few candidates gained full marks for this question. Some candidates demonstrating confusion between which registers hold the actual instruction/data and which hold the memory location address of the instruction/data.
ii	– Contains the address of the instruction (to be accessed in memory)… – …address of instruction sent from PC – Contains the address of the data (to be accessed in memory)… – …address of data sent from CIR	2	**Examiner's Comments** Again, some candidates demonstrated confusion between registers. A common error was 'address of next instruction'.
iii	– Contains the instruction which has been accessed from memory – Contains the data which has been accessed from memory – That is referenced by the MAR / Instruction sent to CIR – acts as a buffer	2	**Examiner's Comments** Although most candidates did state that this register holds data/instructions there was a lack of clarity about where the data/instruction was coming from/going to, hence not clearly explaining the need for the register.
a	**Two from:** ▫ Decodes instructions. [1] ▫ Sends control signals to coordinate movement of data through the processor / execute instruction. [1] ▫Controls buses [1]	2	Accept manages / coordinates / synchronises the FDE cycle for BP 1 and 2 **Examiner's Comments** Some candidates answered this question well, however descriptions in some cases lacked attention to detail with some responses not going beyond '…the control unit tells all the parts of the processor what to do…' which is not creditworthy at this level.

	i	• Gives more cycles per second • More instructions can be executed per second • So the program takes less time to run *(1 per -, Max 2)*	2	Do not accept '…data is processed quickly…' as BP3 **Examiner's Comments** Many candidates achieved some credit on this question but candidates did not achieve full marks due to lack of attention to detail in their description. Many candidates used phrases such as 'processor will run quicker / faster' without describing how a fast clock speed would enable this.
	ii	• More space for data / instructions in cache memory • RAM needs to be accessed less frequently • Accessing cache is quicker than accessing the RAM *(1 per -, Max 2)*	2	**Examiner's Comments** Similarly, the lack of detailed responses limited credit achieved on this question. Many candidates used phrases such as 'large cache means faster processing' without describing how a large cache would enable this.

If you found this useful, drop a follow to help me out!

THANK YOU!

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